

## Research Article

# An Improved Topology of Isolated Bidirectional Resonant DC-DC Converter Based on Wide Bandgap Transistors for Electric Vehicle Onboard Chargers

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Received 20 December 2022; Revised 11 February 2023; Accepted 16 February 2023; Published 2 March 2023

Academic Editor: Anjanee Kumar Mishra

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This article proposes an improved topology for an isolated bidirectional resonant DC-DC converter for electric vehicle (EV) onboard chargers. As opposed to the conventional capacitor-inductor-inductor-inductor-capacitor (CLLLC) resonant converter, the proposed converter's resonant circuit is composed of a capacitor-inductor-inductor-inductor (CLLL) structure, whose inductances, except the capacitor, can be fully integrated with the leakage and mutual inductances of the high-frequency transformer (HF). Therefore, this offers a smaller size, lower costs, minimal power loss, and eventually higher efficiency. Again, the proposed converter design is based on wide bandgap (WBG) transistor switches that operate at MHz-level switching frequency to achieve high power density, high efficiency, and high compactness. A discrete-time proportional integral derivative (PID) controller has been designed using the phase-shifted pulse width modulation (PSPWM) technique to assure closed-loop control of the proposed CLLL converter. The PID controller parameters have been optimized using both the genetic algorithm (GA) and particle swarm optimization (PSO) algorithm and a comparative analysis has been presented between the two algorithms. To achieve fast switching with very little switching loss, the converter is simulated with several wide bandgap (WBG) switching devices. A performance comparison with conventional Si-based switching devices is also provided. A precise power loss model of the semiconductor switches has been devised from the manufacturer's datasheet to achieve a perfect thermal design for the converter. A 5 kW CLLL converter with an input range of 400–460 V direct current (DC) and an output range of 530–610 V DC, and a switching frequency of 1 MHz has been designed and investigated under various loading scenarios. Gallium nitride (GaN) switching device-based designs achieved the highest levels of efficiency among the switching devices. The efficiency of this device is 97.40 percent in charging mode and 96.67 percent in discharging mode.

## 1. Introduction

Bidirectional DC-DC converters (BDCs) are used in a wide range of applications that require bidirectional power transmissions, such as electric vehicles (EVs), renewable energy systems, industrial systems, DC power distribution systems, aerospace power supplies, more electric aircraft (MEA) power supplies, uninterruptible power supplies (UPS), and fuel cell and battery energy storage systems (BESS) [1–8]. These types of high-power high gain BDCs are capable of achieving both DC voltage variation and electrical

isolation. Figure 1 shows a schematic illustration of a standard EV onboard battery charger system, which contains an AC-DC power factor correction (PFC) stage and a bidirectional DC-DC converter (BDC) [9]. The PFC stage is connected to the AC power grid through an EMI filter and a DC link capacitor to achieve unity PFC and AC to pure DC conversion. The BDC connects an EV battery pack with the DC link capacitor to achieve current and voltage regulation as well as galvanic isolation which is essential for V2G applications. These BDCs can power EV battery loads while also providing power feedback to the power grid. Dual active

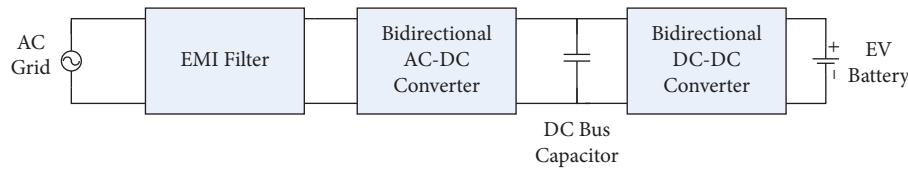


FIGURE 1: Schematic illustration of a standard EV onboard battery charger system.

bridge (DAB) [10, 11] and CLLC [12–16] converters are among the current BDC topologies that have drawn a lot of focus because of the high-frequency (HF) transformers' simplistic and symmetrical architecture on both sides, high efficiency, high conversion ratio, and high power density.

The main benefit of a DAB resonant BDC over a CLLC resonant BDC is the lack of resonant capacitors that need to endure high voltage strains. Contrarily, the CLLC resonant BDC can soft switch in almost any loading situation. With no auxiliary circuit required, these converter's semiconductor switches can achieve zero voltage switchings (ZVS) on the inverter side and zero current switchings (ZCS) on the rectification side, allowing them to use higher switching frequencies.

Several research studies have been carried out to improve the performance of CLLC resonant BDCs for various applications because of the CLLC resonant converter's current popularity and broad application prospects. For instance, Wang et al. [17] developed a novel paralleled CLLC converter technique that distributes system load evenly among the parallel CLLC units. As a consequence, the system power handling capability and power density can be enhanced. In [16], an innovative operation mode analysis was developed to determine the optimum tank parameters for a specific set of circumstances. To build high-power-density resonant converters, it is shown in [18] that increasing the switching frequency from 65 kHz to 1 MHz reduces the overall size of resonant components by almost half. Zong et al. [19] established a double voltage rectification modulation approach that provides a step-up voltage gain to widen the operating voltage range of resonant BDCs. A technique to lessen the electromagnetic interference (EMI) noise generated by the common-mode (CM) CLLC BDCs was put forth by Chu et al. [20]. Consequently, CM chokes can be reduced in size, while the converter power density can be increased. In [15], a WBG switching device-based CLLC converter was designed and evaluated. GaN switching devices have been proven to be the most efficient. The PID controller parameters, nevertheless, are not optimized in this work. However, in symmetrical bidirectional topologies, such as the CLLC converter [12–16], there are at least five resonant elements, whereas, in asymmetric bidirectional topologies, such as the proposed CLLL converter, there are only four resonant elements, which thus helps in reducing the difficulty of parameter design. It also minimizes the design's size and cost. This proposed CLLL resonant network combines all of the advantages of a lower-order resonant converter, by absorbing all parasitic components, and enabling operation at high switching frequencies with minimal switching losses. The resonant inductors can be synthesized

from the HF transformer's leakage inductance and can be fully integrated with the HF transformer. By altering the air gap between the windings and core halves, the leakage inductance can be changed. The loss and the core volume of the converter will be reduced as a result of this integrated transformer. As a result, asymmetric bidirectional topologies are thought to be more flexible and efficient. However, no breakthroughs in the field of asymmetric bidirectional topologies research have been made since it is challenging to develop a parameter design procedure that equips the converter with a similar bidirectional operating characteristic.

Furthermore, passive resonant components account for a sizable portion of the total space of switching converters. The most obvious method for lowering the size of passive components is unquestionably the use of higher switching frequencies. Nonetheless, even partial hard-switching at a higher switching frequency at any switching device can result in significant switching losses, thus degrading the efficiency noticeably and thereby adding to the burden of thermal management. Because of this, this article, which focuses on EV onboard battery charger application areas, uses the CLLL resonant structure as a more practical choice for HF DC/DC conversion without no extra control complexity needed to facilitate soft switching.

Additionally, because of the advancement of recent semiconductor technologies, third-generation WBG semiconductor switching devices such as silicon carbide (SiC) and GaN switching devices have been developed to help BDCs achieve a relatively high switching frequency, high efficiency, and high power density by displacing conventional devices such as silicon MOSFETs and silicon IGBTs. An overall view of the few key material characteristics of these devices is given in [21]. GaN material is a great option for high-voltage and high-frequency applications because it has the highest breakdown voltage, energy bandgap, and electron velocity characteristics, according to the comparative data presented in [21]. Additionally, GaN switching devices feature lower gate charges and on-resistance than Si and SiC switching devices, resulting in lower switching charges and rapid switching transition. Furthermore, rapid switching transition leads to less switching loss. Besides that, GaN switching devices offer a lesser output capacitance, which results in reduced switching loss and makes it simpler to implement ZVS. Other Si and SiC-based switching devices require an antiparallel diode, but GaN 2D electron gas (2DEG) does not require one because it can operate in the third quadrant. It consequently has no reverse recovery loss, which lowers switching loss and reduces EMI noise. Despite having less thermal conductivity than SiC, GaN switching

devices can provide high power densities with efficient cooling approaches. GaN switching devices are therefore capable of maintaining high efficiency during the high-frequency operation among the semiconductor switching devices that are currently available [15].

In this regard, this research focuses on developing a high-performance 5 kW 400–460 V DC input 530–610 V DC output 1 MHz bidirectional isolated asymmetric CLLL resonant DC-DC converter utilizing various switching devices. Efficiency calculations were performed using an exact switching device power loss model. A PSPWM-based discrete-time PID controller has been created to control the output voltage and supervise the bidirectional power conversions. The PSO and GA-based optimization techniques have been used to optimize the PID coefficients. The developed converter was evaluated for different switching devices from major manufacturers during the simulation, with the E-mode GaN high electron mobility transistor (HEMT) offering the highest efficiency when compared to the other semiconductor switches.

## 2. Proposed Bidirectional CLLL Converter Operation Principle

The schematic of the proposed isolated bidirectional asymmetric resonant CLLL converter is shown in Figure 2. As can be seen, it employs fewer passive elements than conventional CLLLC converters [15]. This results in high efficiency and power density, which are discussed in detail in the section “Results and Discussions.”

Both charging (G2V, or grid to vehicle) and discharging (V2G, or vehicle to grid) modes are possible with the converter. Two full-bridge converters with four switches each make up this CLLL converter. To accomplish inversion, the S14, as well as S23 switches, are activated in the forward direction at 50% duty cycle. S58 and S67 will achieve rectification with their antiparallel diodes. GaN transistors have inherent reverse conduction capabilities, hence antiparallel diodes are not necessary when using them as switching devices. Only the reverse conduction of Si, SiC MOSFET, and IGBT transistors necessitates antiparallel diodes. In one operation period, the proposed CLLL resonant converter has six stages. The driving circuit's operational scenarios are identical in both forward and backward directions; only the resonant components differ. As a result, the converter's operating principles are essentially identical in both directions, and only one operating direction needs to be investigated. The forward operation principle is discussed in detail in [22], so it will not be discussed further in this paper. Following a thorough examination of the operational procedures, it is revealed that the CLLL resonant DC-DC converter can achieve ZVS on primary-side semiconductor switches as well as ZCS on secondary-side semiconductor switches.

## 3. Design of the Proposed Isolated Bidirectional CLLL Resonant Converter

The converter design includes finding the turns ratio of the transformer ( $n$ ), formulating the magnetizing inductance ( $L_m$ ), capacitances ( $C_1$ ), and inductances ( $L_1$  and  $L_2$ ), as well as developing a PSPWM-based discrete-time PID controller.

**3.1. Transformer's Turns Ratio Design.** Resonant BDCs are most efficient at the self-resonant frequency,  $f_r$ . As a result, the converter ought to operate at this frequency under typical operating circumstances. The transformer's turns ratio can then be determined as

$$n = \frac{N_1}{N_2} = \frac{V_{in-nom}}{V_{o-nom}}, \quad (1)$$

where  $N_1$ ,  $N_2$ ,  $V_{in-nom}$ , and  $V_{o-nom}$  represent the transformer's primary and secondary turns ratios, and nominal input and output voltages, respectively.

**3.2. Resonant Components Design.** Figure 3 displays the CLLL converter's equivalent circuit model in both directions. The components of the resonant tanks are  $L_1$ ,  $L_2$ ,  $L_m$ , and  $C_1$ . When the converter is operating at its self-resonant frequency, the total impedance is pure resistance. As a result, at self-resonant frequency, the converter's reactive impedance should be zero. The following equation can be derived from Figure 3:

$$-j\frac{1}{\omega_r C_1} + j\omega_r L_1 + \frac{j\omega_r (L_m n^2 L_2)}{L_m + n^2 L_2} = 0. \quad (2)$$

By simplifying equation (2), the self-resonant frequency can be obtained, as shown in the following equation:

$$f_r = \frac{1}{2\pi \sqrt{C_1 (L_1 + (L_m n^2 L_2 / L_m + n^2 L_2))}}. \quad (3)$$

Let  $R_e$ ,  $L_2'$  be the corresponding equivalent  $R_o$ ,  $L_2$  of the CLLL converters and here,  $R_o$  stands for the converter's output load resistance. It is possible to calculate the equivalent load resistance by using the fundamental harmonic approximation (FHA) technique. For the G2V (battery charging) mode,  $L_2'$  and  $R_e$  of the converter can be calculated as follows [15]:

$$\begin{aligned} L_2' &= n^2 L_2, R_e, \\ c &= \frac{8n^2}{\pi^2} R_o. \end{aligned} \quad (4)$$

The parameters for the V2G (battery discharging) mode will be the same, and they are as follows [15]:

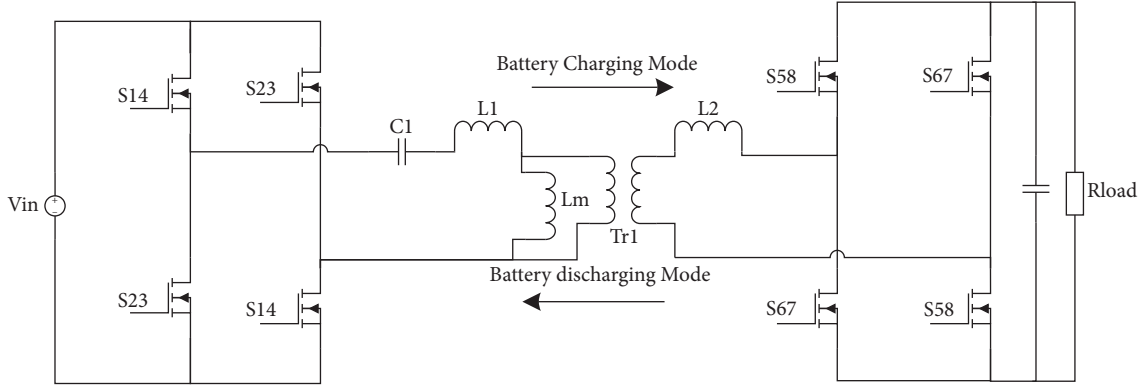


FIGURE 2: Schematic of the proposed isolated bidirectional CLLL resonant DC-DC converter.

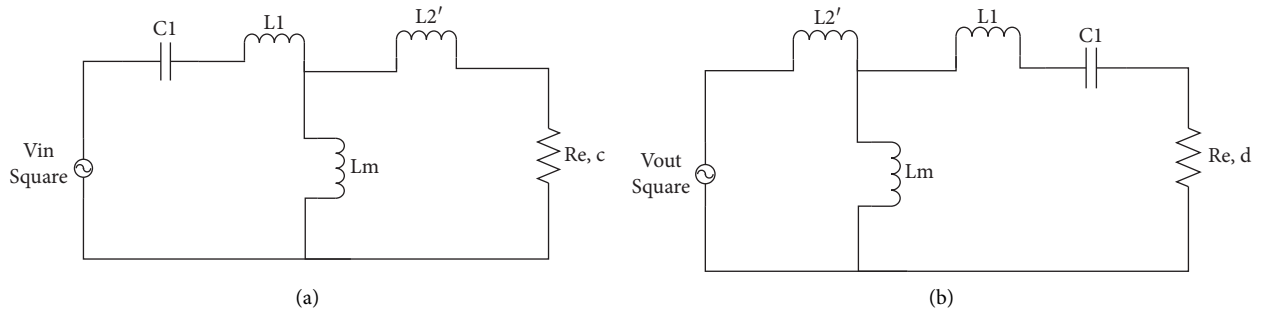


FIGURE 3: Schematic of the proposed converter's equivalent circuit model in (a) forward power flow mode and (b) reverse power flow mode.

$$L_2' = \frac{L_2}{n^2}, \text{Re}, \quad (5)$$

$$d = \frac{8}{n^2 \pi^2} R_o.$$

By keeping the current flowing through primary-side switches negative at the time of turn-on, ZVS in these switches can be ensured. The primary current of the converter ought to be able to completely charge and discharge the output capacitors of the primary switches during the dead time ( $t_{\text{dead}}$ ). The magnetizing inductance ( $L_m$ ) and the length of the dead time determine the amount of this current. Therefore, the primary side switches' ZVS is controlled by the magnetizing inductance ( $L_m$ ), output capacitance of switching devices ( $C_{\text{oss}}$ ), operating frequency, and dead time ( $t_{\text{dead}}$ ). This converter performs in dead time such as an LLC resonant DC-DC converter [23]. This allows the magnetizing inductance to be expressed in a manner that is similar to that of the full-bridge LLC resonant DC-DC converter. Thus, the expression [15] is

$$L_m \leq \frac{t_{\text{dead}}}{16 C_{\text{oss}} f_{s, \text{max}}}, \quad (6)$$

where  $f_{s, \text{max}}$  denotes the highest switching frequency of the proposed converter.

Under various load conditions, a relatively low magnetizing inductance ( $L_m$ ) guarantees ZVS in primary-side switching devices. On the other hand, ( $L_m$ ) can never be set

too low. Too little ( $L_m$ ) would cause the magnetizing current to be extremely high, which would result in significant conduction losses, higher primary-side capacitor peak voltage requirements, and higher apparent power requirements for switching devices. A low magnetizing current is produced by a high magnetizing inductance, but the converter's voltage gain is constrained. Consequently, the magnetizing inductance ( $L_m$ ) should not be too high.

The dead time ( $t_{\text{dead}}$ ) between switching devices has an impact on the ZVS range as well. ZVS will be easier to achieve for a broad range of input and output voltages with long dead time ( $t_{\text{dead}}$ ). Additionally, by uplifting the inductance with a lengthy dead time ( $t_{\text{dead}}$ ), the magnetizing current could be decreased. On the other hand, a relatively high dead time ( $t_{\text{dead}}$ ) will cause a high primary RMS current because there will be no transfer of energy during the dead-time duration. All of these issues must be kept in mind when designing the magnetizing inductance, ( $L_m$ ) of the proposed converter.

Figure 4 depicts the fluctuation of the converter voltage gain over a range of normalized frequencies ( $f_r/f_s$  ratio) with varied loading circumstances, i.e., different quality factors,  $Q = \sqrt{L_1/C_1}/R_e$ . As a result, the output voltage can be regulated by modifying the converter's switching frequency  $f_s$ . Within a suitable switching frequency range, the converter can function in the inductive area (as illustrated in Figure 4), where the switch voltage leads the tank current waveform, ensuring that the voltage returns to zero before the current rises and so ensuring ZVS.

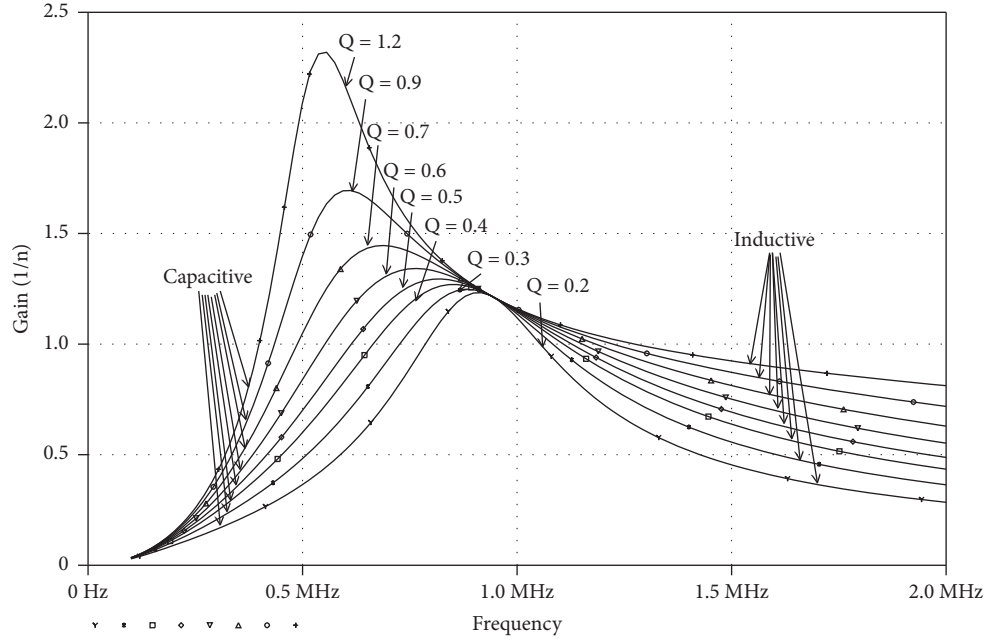


FIGURE 4: Gain waveforms of CLLL converter for different loading conditions.

**3.3. PSPWM-Based Discrete-Time PID Controller Design.** The proposed discrete-time PID controller's block schematic, which is based on PSPWM, is provided in the following Figure 5.

The three main components of the controller are the “ZOH” (zero order hold) block, the “discrete-time PID controller transfer function” block, and the “phase shift PWM” block. The difference signal between the reference and actual output voltage levels is sampled by the “ZOH” block and stored there. The output voltage is then stabilized and regulated by the “discrete-time PID controller transfer function” block using proportional, integral, and derivative control. The following equation can be used to represent the transfer function of the discrete-time PID controller in the Z domain [15]:

$$C(z) = K_p + \frac{K_i T_s z}{z-1} + \frac{K_d N (z-1)}{(1+NT_s)z-1}, \quad (7)$$

where  $K_p$ ,  $K_i$ , and  $K_d$  denote the proportional, integral, and derivative gains of the proposed PID controller, respectively,  $T_s$  denotes the sampling period, and  $N$  denotes the parameter of the first-order filter on the derivative term.

Once more, equation (7) can be changed to yield the following [15] expression:

$$C(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}}, \quad (8)$$

which has the following coefficients:

$$b_0 = K_p (1 + NT_s) + K_i T_s (1 + NT_s) + K_d N,$$

$$b_1 = -(K_p (2 + NT_s) + K_i T_s + 2K_d N), \quad b_2 = K_p + K_d N,$$

$$a_0 = (1 + NT_s), \quad a_1 = -(2 + NT_s), \quad a_2 = 1.$$

(9)

However, the PID controller gains in [15] are determined by trial and error, which is not an optimized process. As a result, the converter is incapable of effectively stabilizing and regulating the output voltage. Because of this, efforts have been made in this work to optimize the PID controller gains. Two optimization techniques, genetic algorithm (GA) [24, 25] and particle swarm optimization (PSO) [26–28], were used to optimize the PID controller gains. Their step responses were also compared for the stability analysis. Because PLECS excels at the power electronics system level simulation and MATLAB is required for controller optimization, MATLAB and PLECS co-simulation were used in this work. In the GA, the search for the optimal solution space mimics the way natural selection drives biological evolution. It repeatedly adjusts a population of individual solutions and, at each step, picks people from the current population to be parents and utilizes them to generate offspring for the upcoming generation. The population progresses toward an optimal solution over subsequent generations by achieving the best fitness value. ITAE (integral of time weighted absolute error) is employed as the fitness function in this case. The pseudocode for the GA algorithm (see Algorithm1) is as follows:

```

(1) Initialize random population;
(2) Evaluate the population;
(3) Generation = 0;
(4) While the termination criterion is not satisfied do
(5)   Generation = generation + 1;
(6)   Select elite individuals with lower fitness scores;
(7)   Perform crossover with probability crossover;
(8)   Perform mutation with probability mutation;
(9)   Evaluate the population;
(10) End while
(11) Return the best individual during the evolution;

```

ALGORITHM 1: Pseudocode of the genetic algorithm [24].

Figure 6 shows the minimum observed fitness value as the genetic algorithm solver progresses. The optimized controller parameter by the genetic algorithm is given as

$$\begin{aligned}
 K_p &= 11.0956, \\
 K_i &= -12.7484, \\
 K_d &= -3.8236, \\
 N &= 3.0057.
 \end{aligned} \tag{10}$$

PSO, like GA, is a population-based algorithm. The main advantage of the PSO is that it can find the best solution with the least amount of computation. This PSO algorithm is inspired by the swarming flocks of birds or insects. Based on an objective function, each particle is drawn to some extent to the best place it has located this far, as well as the best location found by any member of the swarm. After a few iterations, the population may congregate around a single site, a few spots, or continue to migrate.

The pseudocode for the PSO algorithm (see Algorithm 2) is as follows:

Figure 7 shows the minimum observed fitness value as the genetic algorithm solver progresses. The optimized controller parameter by the genetic algorithm is given as

$$\begin{aligned}
 K_p &= -0.7053e04, \\
 K_i &= -0.0555e04, \\
 K_d &= 0.2595e04, \\
 N &= -0.0664e04.
 \end{aligned} \tag{11}$$

The step response performance of these two optimization algorithms is compared in Table 1. According to Table 1, both optimization techniques performed similarly and satisfactorily. In some aspects, the GA PID controller performed better than the PSO PID controller, which converged faster with less computation. As a result, when it comes to fast computation, the PSO PID controller outperforms the GA PID controller.

As shown in Figure 5, the “Phase Shift PWM” block uses the PSPWM technique in the output signal of the PID controller. It sends the pulse signal that switching devices require in order to stabilize and regulate the output voltage signal. Figure 8 shows the block diagram of the PWM

subsystem. The PID output signal is compared with the other two sawtooth PWM carrier signals with a 180-degree phase shift between them to generate the phase-shifted PWM control signal waveform for the switches. The final gate signals for the switches are generated by the SR flip-flop block. The internal block diagram of the SR flip-flop is shown in Figure 9. It was built with a pair of cross-coupled NOR logic gates.

In the G2V (battery charging) mode of the proposed converter, the input voltage range is 400–460 V, while the output voltage range is 530–610 V. Correspondingly, in the V2G (battery discharging) mode, the input voltage range is 530–610 V, while the output voltage range is 400–460 V. The nominal operating frequency in the charging and discharging modes is 1 MHz. The resonant frequency is set at 1 MHz. To step up the input voltage, the transformer turns ratio,  $n$  is set to  $400/530 \cong 0.8$  according to equation (1). Load resistance can be calculated from the equation  $V_o^2/P$  equation, where  $V_o$  and  $P$  is the expected output voltage and power, respectively. From equations (3)–(6), the resonant parameters  $L_1$ ,  $L_2$ ,  $L_m$ ,  $C_1$ , and  $C_2$  can be determined, producing the following results:

$$\begin{aligned}
 L_1 &= 3.49 \mu H, \\
 L_2 &= 4.62 \mu H, \\
 L_m &= 21.5 \mu H, \\
 C_1 &= 3.91 nF.
 \end{aligned} \tag{12}$$

## 4. Results and Discussions

To validate the proposed system, simulations using the PLECS Standalone software and MATLAB/Simulink were performed. Figure 10 depicts the peak efficiency curves of the proposed CLLL converter using GaN E-HEMT devices under varying load conditions for both G2V and V2G modes. The proposed CLLL converter has a higher efficiency in the charging or G2V mode than in the discharging or V2G mode. In both charging and discharging modes, the proposed converter has good efficiency over a wide load range.

Figure 11 depicts the peak efficiency, output voltage, and output current vs. switching frequency for the proposed converter in both G2V and V2G modes. The peak efficiency

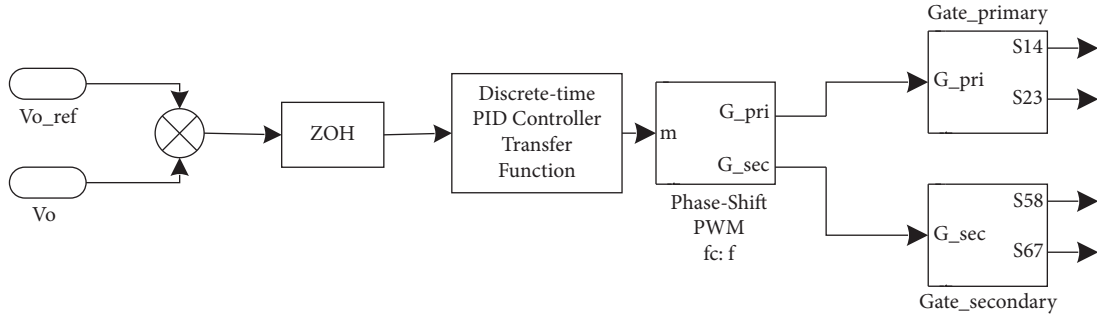
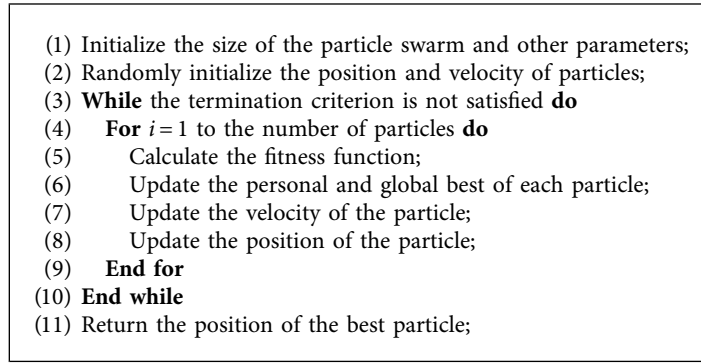


FIGURE 5: Block schematic for the proposed PID controller [15].



ALGORITHM 2: Pseudocode of the PSO algorithm [26].

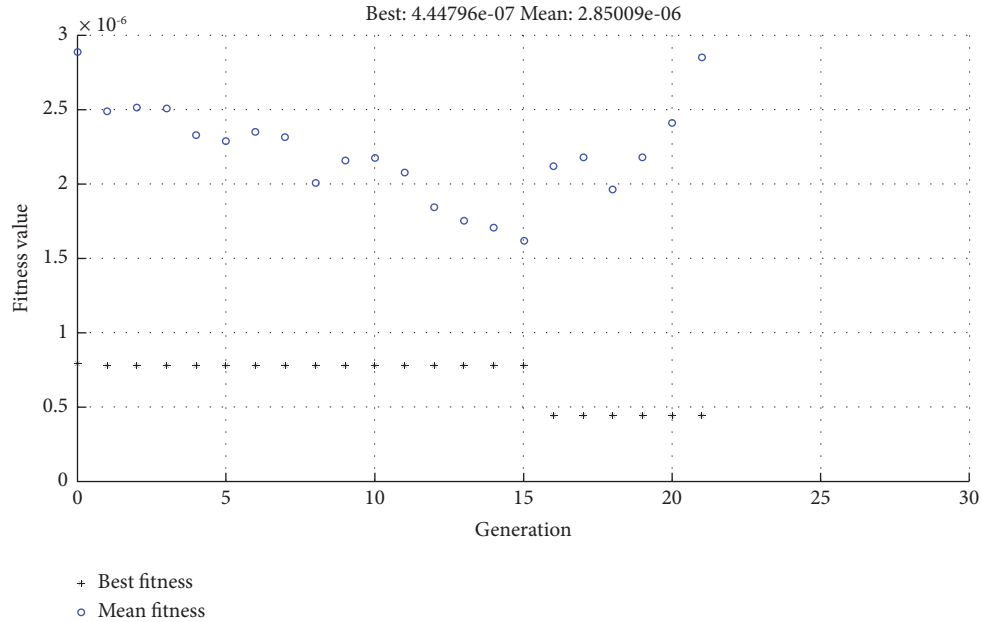


FIGURE 6: Fitness value of the genetic algorithm optimization.

was achieved at 1 MHz switching frequency since it is the resonant frequency and accomplishes ZVS turn-on at this frequency. That is why it has the highest efficiency at this frequency. The peak efficiency of the converter began to drop below or above this switching frequency. Because of the same reason, the output voltage and output current are at

their peak at 1 MHz frequency and then begin to decline below or above that level.

While utilizing automotive standard switching devices built with GaN, SiC, and Si, the performance of the proposed converter was also assessed. PLECS device models, including turn-on loss, turn-off loss, conduction loss, and thermal

TABLE 1: Step response performance of the GA and the PSO PID controller.

| Step response characteristics | Plant with GA PID controller | Plant with PSO PID controller |
|-------------------------------|------------------------------|-------------------------------|
| Rise time                     | $1.5265e-05$                 | $1.5260e-05$                  |
| Transient time                | $8.2185e-05$                 | $8.2388e-05$                  |
| Settling time                 | $8.2185e-05$                 | $8.2388e-05$                  |
| Settling min                  | 480.4168                     | 480.4168                      |
| Settling max                  | 648.2221                     | 648.2221                      |
| Overshoot                     | 22.0123                      | 22.0997                       |
| Undershoot                    | 0                            | 0                             |
| Peak                          | 648.2221                     | 648.2221                      |
| Peak time                     | $3.0107e-05$                 | $3.0107e-05$                  |
| ITAE                          | $4.448e-07$                  | $2.9662e-07$                  |

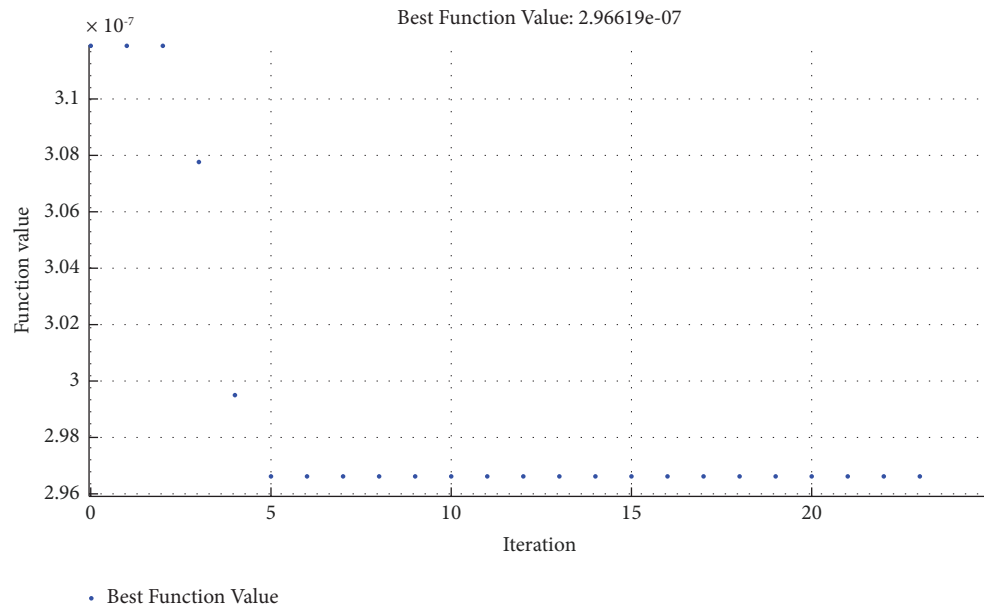


FIGURE 7: Fitness value of the PSO algorithm.

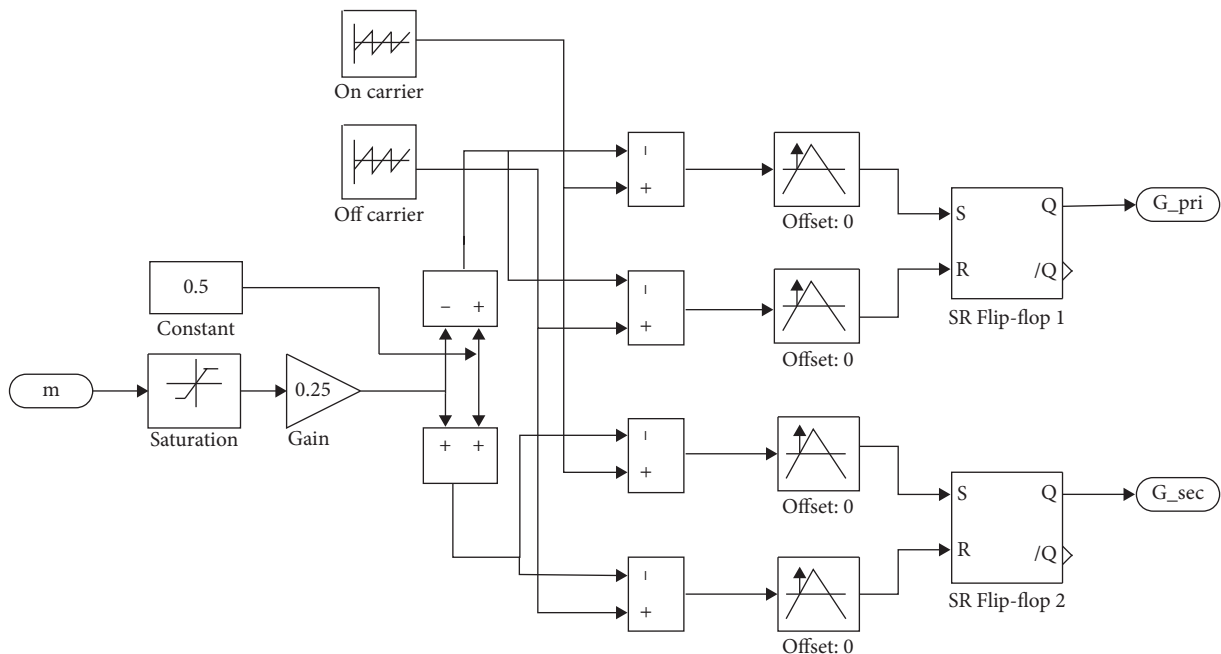


FIGURE 8: Phase shift PWM block diagram.

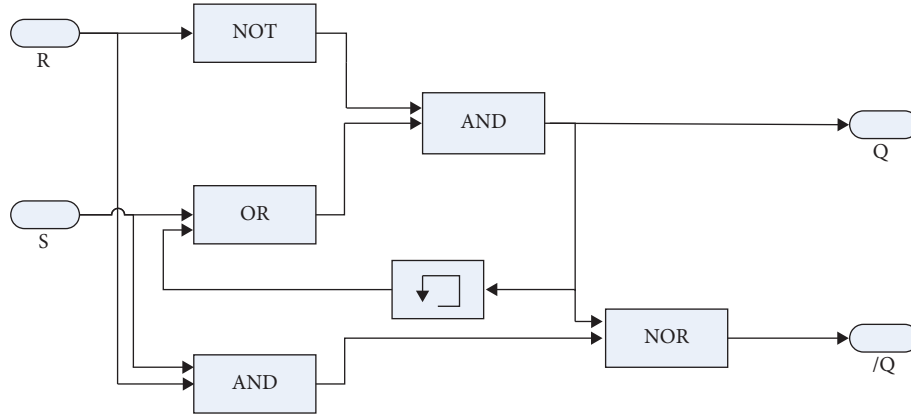


FIGURE 9: SR flip-flop block diagram.

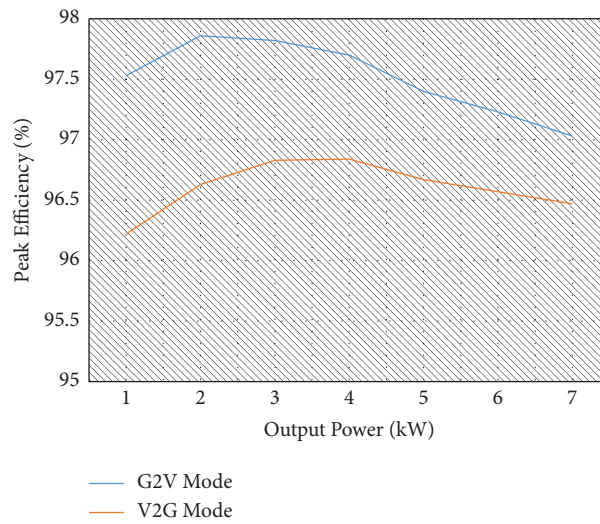


FIGURE 10: Efficiency curves of CLLL converter utilizing GaN devices under varying load conditions.

impedance data, were obtained from various manufacturers' datasheets for practical loss and efficiency calculations. The subsections that follow describe the performance of these devices using this converter.

**4.1. E-Mode GaN HEMT-Based CLLL Converter from GaN Systems Inc [29].** In this work, a GaN switching device made by GaN Systems Inc., the GS-065-150-1-D2 [29], has been used. The GS-065-150-1-D2 is a 650 V, 150 A, and 10 mΩ on-resistance enhancement-mode GaN-on-silicon power transistor. It offers zero reverse recovery loss and an extremely high switching frequency (>10 MHz) [29]. In charging mode, the converter's simulated waveforms are shown in Figure 12. It is clear that the switches turn on ZVS. The ripple in the output voltage is almost zero. The circuit yields comparable outcomes in discharging mode.

**4.2. E-Mode Planar SiC MOSFET-Based CLLL Converter from Cree Inc [30].** For this work, the SiC switching device was an n-channel enhancement planar MOSFET with the model number C3M0060065D manufactured by Cree Inc [30]. This

650 V and 29 A SiC MOSFET has a fast intrinsic diode with a small reverse recovery ( $Q_{rr}$ ), fast switching with small capacitances, and high blocking voltage with low on-resistance (60 mΩ) [30]. Figure 13 displays the simulated waveforms for this SiC device's charging mode.

The waveforms show the ZVS of the switching device. In comparison to the prior GaN device, the output voltage and output current both are marginally lower. Like the GaN switching device, the output voltage ripple is almost zero. The proposed converter's discharging mode results in waveshapes similar to those of the GaN.

**4.3. Trench Structure SiC MOSFET-Based CLLL Converter from ROHM Semiconductor [31].** A trench gate SiC MOSFET with a 650 V, 39 A, and 60 mΩ operating voltage that is designed for high-efficiency server power supplies, renewable energy systems, and EV chargers is the SCT3060AR from ROHM Semiconductors [31]. The first company to mass-produce trench-type MOSFETs, with increased efficiency while consuming less power than traditional SiC MOSFETs, was ROHM, a SiC technology pioneer and

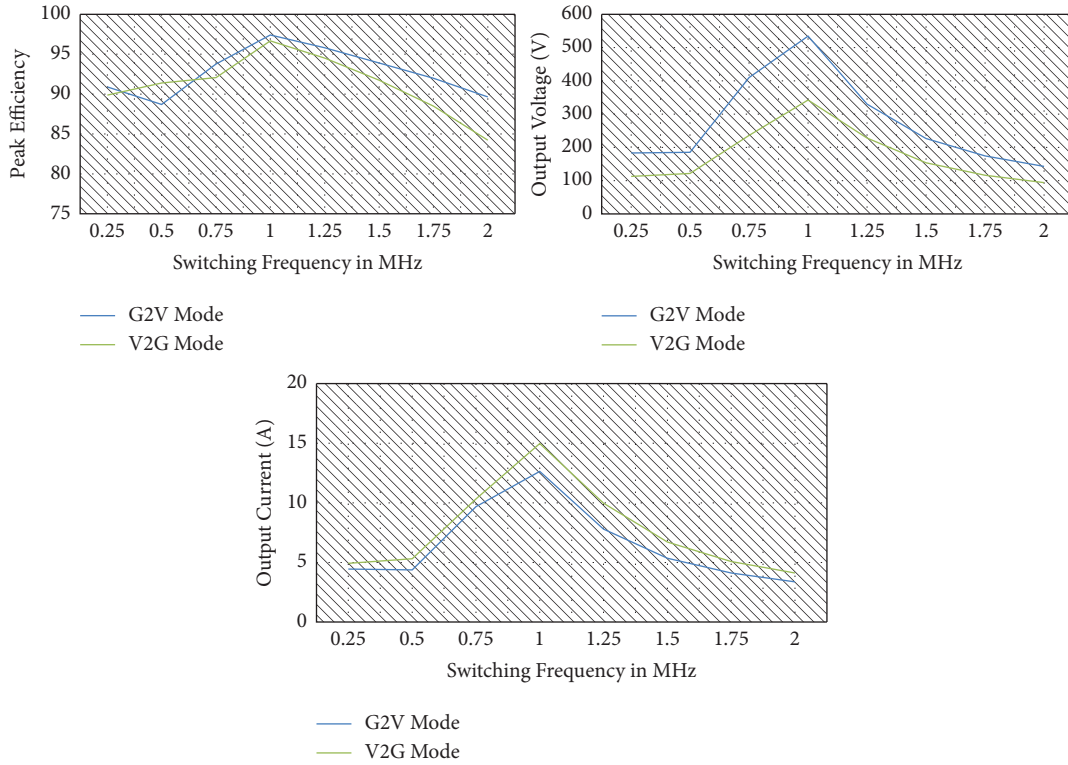


FIGURE 11: Peak efficiency, output voltage, and output current versus operating switching frequency for the converter operating in the G2V and V2G mode.

market leader. The performance of the converter with this device in charging mode is shown in Figure 14. It is obvious from the waveforms that this device also displays a ZVS turn-on. In comparison to the previous planar SiC device, the output voltage and current are higher. The trench SiC device performs better than the previous planar SiC device as a result. Additionally, this device's output voltage and current closely resemble those of the previous GaN device. Similar outcomes are produced by the converter in discharging mode.

**4.4. Si Power Transistor-Based CLLL Converter from Infineon Technologies [32].** The SPP20N60C3 [32] Si power transistor from Infineon Technologies has a voltage rating of 650 V, a current rating of 20.7 A, and an on-resistance of 190 mΩ. This device has better transconductance, a higher peak current capability, and a very low gate charge than other Si power transistors [32]. When using this device in charging mode, the performance of the designed converter is shown in Figure 15. The output voltage has almost no ripple. The

switching device offers a ZVS turn-on in this instance as well. The converter's performance is similar in discharging mode.

**4.5. Field Stop Trench Si IGBT-Based CLLL Converter from ROHM Semiconductor [33].** The RGW60TS65DHR [33] from ROHM Semiconductor is a 650 V 30 A Si field stop trench IGBT. This device has a fast recovery diode (FRD) built in for reverse conduction, low collector-emitter saturation voltage, and a low switching loss [33]. The converter's operation with the device in charging mode is shown in Figure 16. The output voltage is also free from a ripple in this instance. It guarantees that ZVS is activated as well. Also, the converter functions similarly when discharging.

## 5. Comparative Analyses

The loss comparison of the proposed converter in terms of total conduction loss and total switching loss across the primary and secondary switches using the GaN, SiC, and Si-

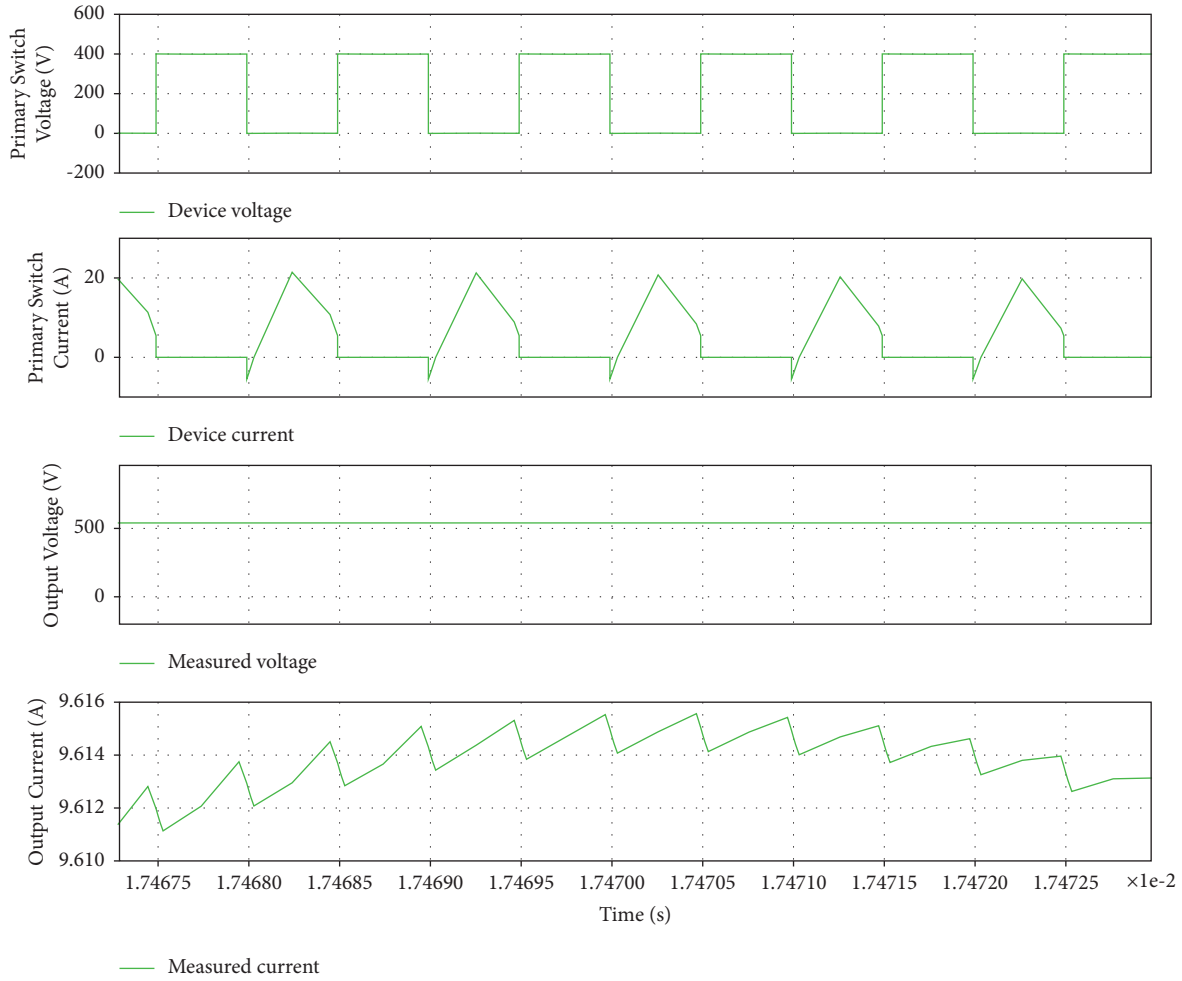


FIGURE 12: E-mode GaN HEMT enabled converter simulated waveforms.

based switching devices is shown in Table 2. According to Table 2, the GaN System's E-mode GaN HEMT switch outperformed the other Si and SiC-based switching devices in terms of total switching loss across the primary and secondary switches.

Si IGBT performed better than the other GaN, Si, and SiC-based switching devices in terms of total conduction loss, but it performed the worst in terms of total switching loss, which is equal to 305.64 W. So, when we consider the two losses of the switches, we can clearly see that the GaN System's E-mode GaN HEMT is the best switching device because its total conduction and switching loss sums to 176.64 W ( $167.79 \text{ W} + 8.85 \text{ W} = 176.64 \text{ W}$ ), which is significantly lower than the other switching devices. As a result,

among the SiC and Si-based semiconductor switching devices, E-mode GaN HEMT made by GaN Systems Inc. is the best choice as a switching device for the proposed CLLL converter.

The overall effectiveness of the proposed CLLL converter using various switching devices is summarized in Figure 17. The designed CLLL converter, which uses a GaN E-mode HEMT as a switching device, has the highest G2V efficiency (97.4%), as shown in Figure 17(a). GaN devices perform better than SiC and Si MOSFET-based designs, but Si IGBT-based designs perform the worst. According to Figure 17(b), the situation in battery charging mode (G2V) is comparable to that in battery discharging (V2G) mode. When different switching devices are used, the designed converter's output

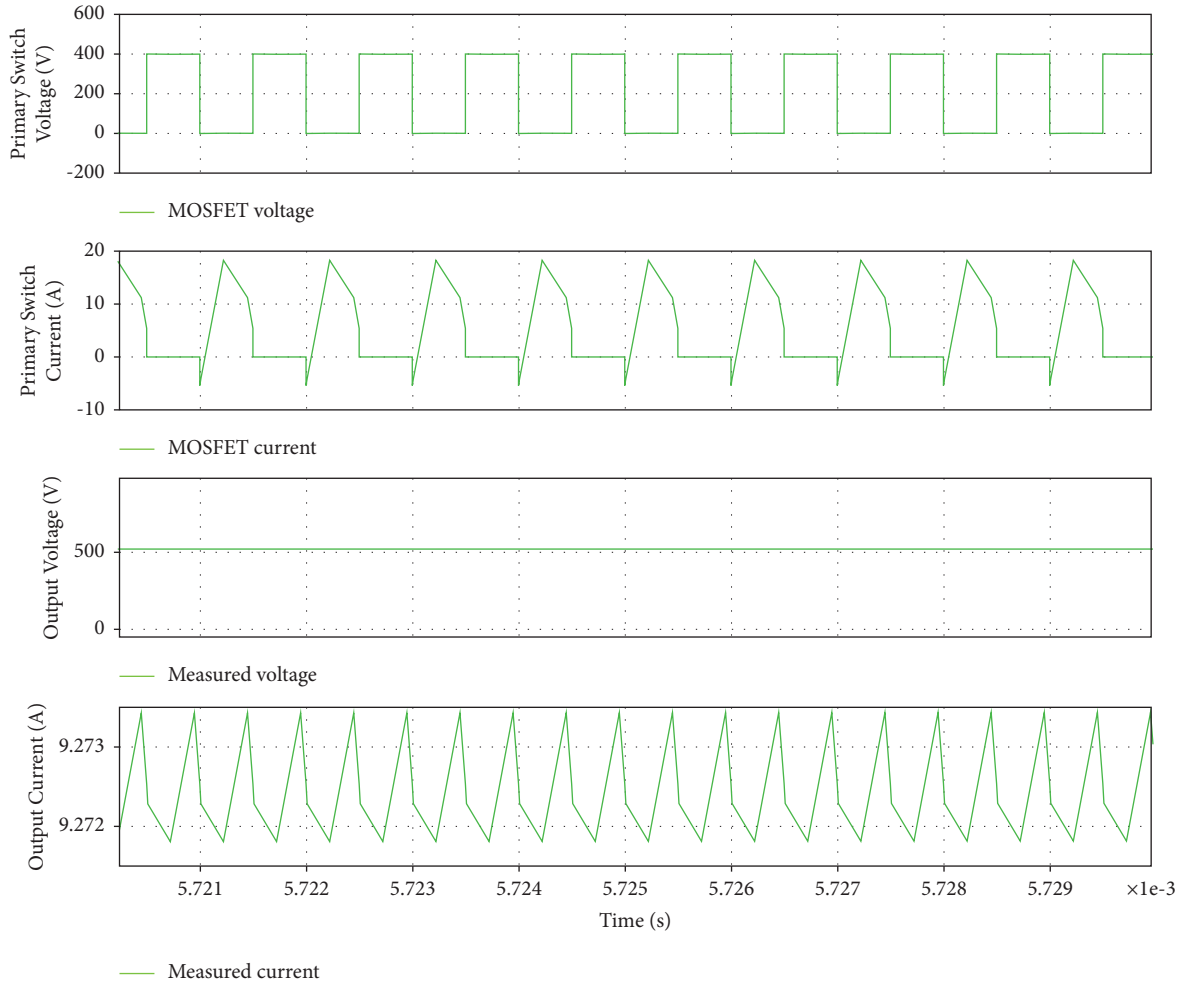


FIGURE 13: Simulated waveforms of the proposed converter with planar SiC device.

current is shown in Figure 17(c). The lowest and highest output currents were attained by Cree Inc.'s SiC and ROHM Semiconductor's IGBT, respectively. To sum up, an optimized converter solution can be provided by GaN-based switches made by GaN Systems Inc.

Moreover, as shown in Table 3, in terms of the highest G2V (battery charging mode) efficiency (%), highest V2G (battery discharging mode) efficiency (%), and peak output power (kW), this converter outperforms the GaN-based CLLC resonant DC-DC converter proposed in [15], the GaN-based CLLC resonant DC-DC converter proposed in [34], the GaN-based multi-CLLC resonant DC-DC converter proposed in [35], and the GaN-based asymmetric CLLC resonant DC-DC converter suggested in [36]. The highest G2V efficiency (97.4%) and highest V2G efficiency (96.67%)

of the suggested converter are both mostly higher than those of the findings presented in [15, 34–36]. The proposed converter surpasses [34–36] by achieving a peak output power of 5 kW. The designed converter ensures a high switching frequency (1 MHz), which is higher than that of [34, 36] and leads to high efficiency and high compactness. To minimize the converter's size and cost, a lower number of resonant elements were chosen for the converter design. In comparison to the proposed converter, [15, 34, 35] utilized a higher number of resonant elements. Additionally, in the resonant elements of the proposed converter, without the capacitance, the two resonant inductances can be integrated with the HF transformer's leakage inductances. Therefore, the proposed converter can result in a more compact design than the converter presented in [15, 34–36]. The GaN-based

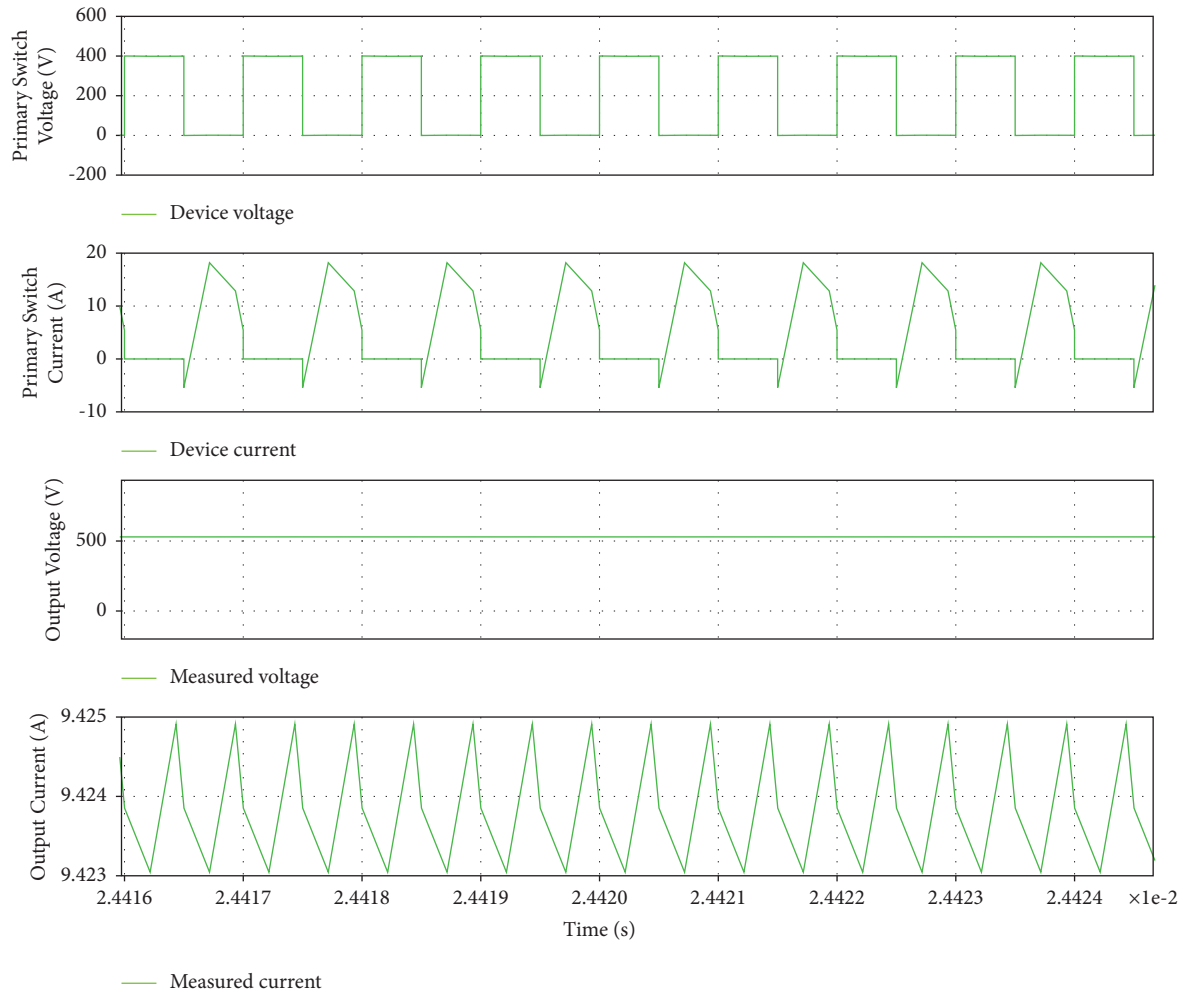


FIGURE 14: Simulated waveforms of the converter with trench SiC device.

switching devices were used in all of the converter structures. Only the structure of the resonant converter differs. Furthermore, an optimized PID controller based on PSO and GA algorithms is proposed in the designed CLLL converter,

which improves the converter's ability to effectively stabilize and regulate output voltages in the presence of noise disturbances compared to the work presented in [15]. Therefore, it is possible to infer that the proposed isolated



FIGURE 15: Simulated waveforms for the Si power transistor-based converter.

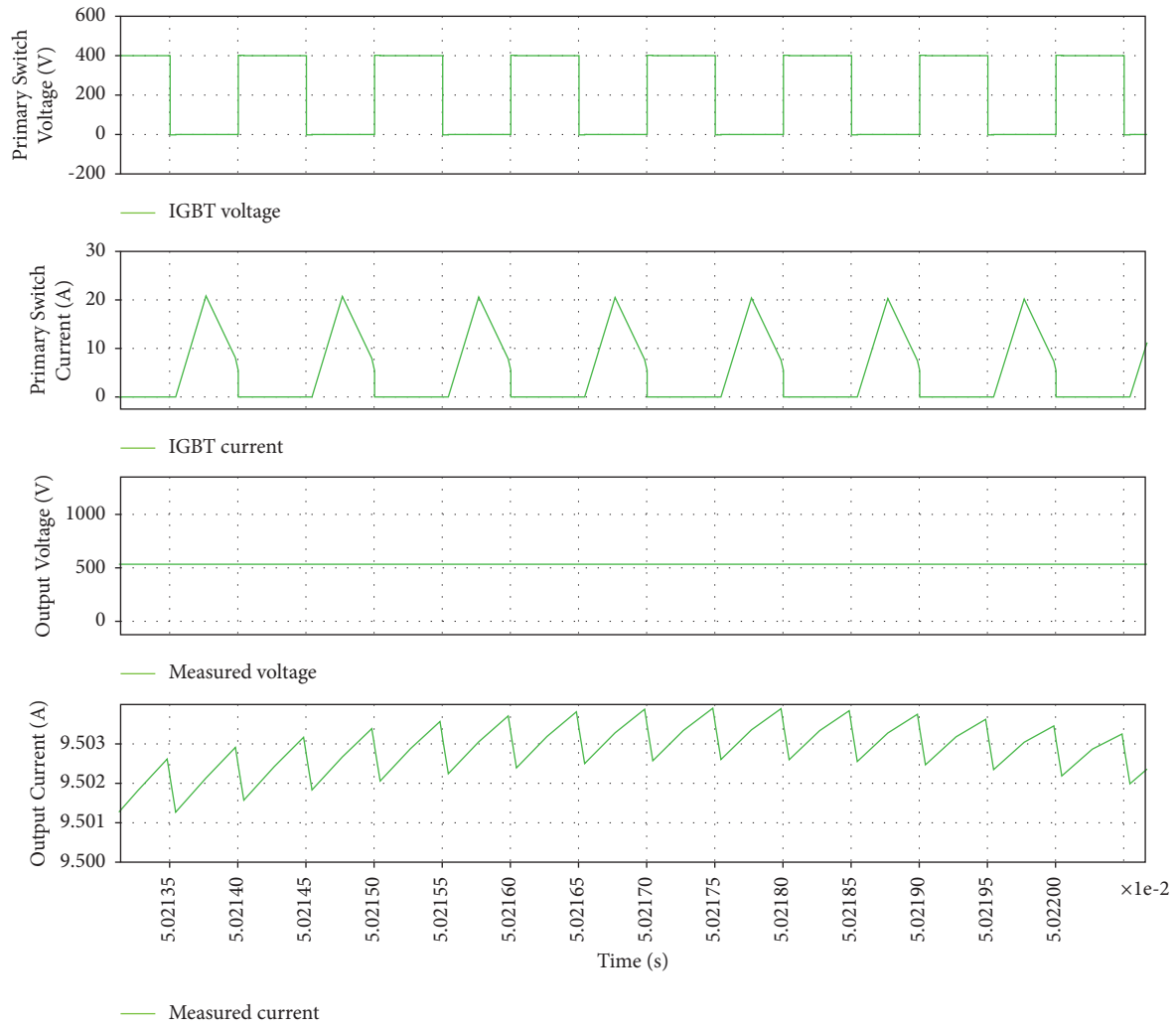


FIGURE 16: Simulated waveforms of the proposed converter with trench IGBT devices.

TABLE 2: Loss comparison of the proposed converter.

| Utilized switching device                              | Total conduction loss (W) | Total switching loss (W) |
|--------------------------------------------------------|---------------------------|--------------------------|
| E-mode GaN HEMT by GaN Systems Inc [29]                | 167.79                    | 8.85                     |
| E-mode planar SiC MOSFET by Cree Inc [30]              | 182.82                    | 61.88                    |
| Trench structure SiC MOSFET by ROHM Semiconductor [31] | 124.98                    | 121.55                   |
| Si power MOSFET by Infineon Technologies [32]          | 158.40                    | 58.70                    |
| Field stop trench Si IGBT by ROHM Semiconductor [33]   | 73.40                     | 305.64                   |

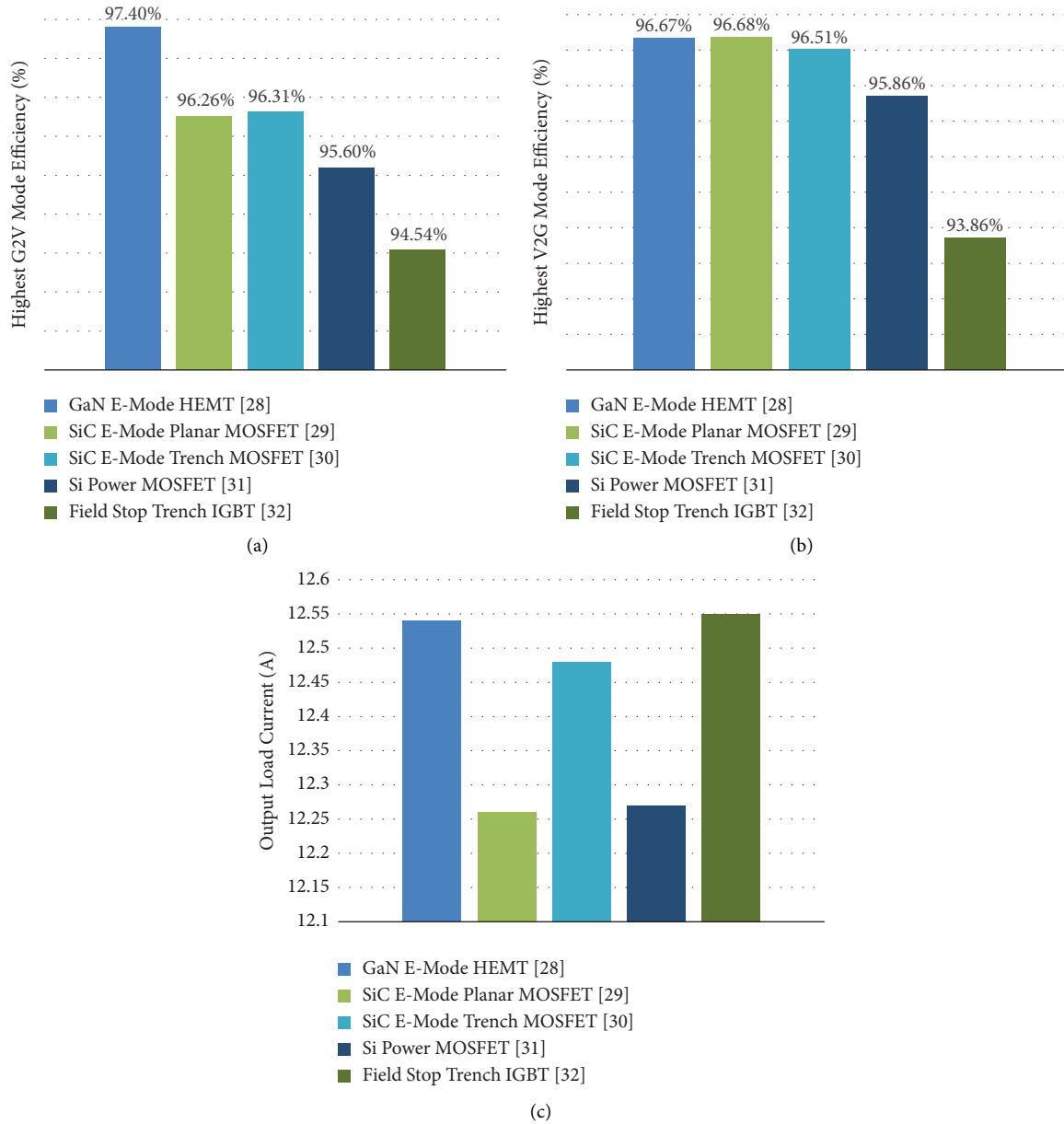


FIGURE 17: Comparative analysis of the proposed converter in terms of (a) highest G2V (charging) mode efficiency, (b) highest V2G (discharging) mode efficiency, and (c) output load current.

TABLE 3: Performance comparison with existing topologies.

| Criteria                   | [15] | [34]  | [35] | [36]  | This work |
|----------------------------|------|-------|------|-------|-----------|
| Max $V_{bus}$ (V)          | 465  | 540   | 400  | 400   | 610       |
| Switch technology          | GaN  | GaN   | GaN  | GaN   | GaN       |
| Switching frequency (MHz)  | 1    | 0.391 | 1    | 0.5   | 1         |
| Resonant elements          | 5    | 5     | 8    | 4     | 4         |
| Highest G2V efficiency (%) | 97.2 | 95.2  | 92.2 | 97.02 | 97.4      |
| Highest V2G efficiency (%) | 97   | 95.7  | 92   | 95.96 | 96.67     |
| Peak output power (kW)     | 5    | 1     | 0.4  | 0.4   | 5         |

bidirectional CLLL resonant converter structure is superior to those discussed in [15, 34–36] in terms of performance.

## 6. Conclusion

This article describes the detailed design process for an improved isolated bidirectional resonant converter that uses a CLLL resonant structure. In comparison to the conventional isolated bidirectional CLLLC resonant converter, this resonant converter provides better performance and a more compact design. The converter's input and output voltage ranges are 400–460 V DC and 530–610 V DC, respectively, at a switching frequency of 1 MHz, and it has been developed and tested with a 5 kW rated power. This converter makes it possible to transfer power in both directions while also operating at high frequencies and high efficiency. The switching loss in this MHz scenario is significantly reduced by this CLLL converter architecture, which guarantees soft switching of both primary and secondary semiconductor switching devices. The PSO and GA-based algorithms are used to design the optimal PID controller that is suggested in this paper. The proposed converter is examined in-depth in this paper, along with a comparison of the high voltage, high current, and low on-resistance semiconductor switching devices that can be used with it. Because GaN switching devices have low switching loss and zero reverse recovery loss, the proposed CLLL converter employing GaN-based switching devices from GaN Systems Inc. has the highest converter efficiency of any switching device currently on the market. The least efficient designs are those based on Si, followed by SiC-based designs. This GaN-based CLLL converter has peak efficiencies of 97.40 percent for charging and 96.67 percent for discharging at full load. The proposed converter operates at a high frequency (1 MHz), which results in minimal passive resonant component sizes. As a result, this proposed converter can achieve a higher power density. Therefore, this isolated bidirectional asymmetric CLLL resonant DC-DC converter based on the GaN switching devices can be very effective for the EV onboard charger systems due to its high performance and compact design.

## Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

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